Amendments to the Claims:

Please cancel claim 2.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A semiconductor memory device, comprising:

~~having~~ an output driver in which a first NMOS transistor and a second NMOS transistor are connected in series, a drain of the first NMOS transistor is connected to an output pad, and the source of the second NMOS transistor is connected to a ground voltage~~, wherein:~~;

a first driving circuit for receiving a reference voltage and generating a first internal voltage, the [[a]]first internal voltage [[is]]being applied to the gate of the first NMOS transistor; and

a second driving circuit for receiving an internal supply voltage and data and generating a second internal voltage, the second internal voltage being [[is]] applied to the gate of the second NMOS transistor; [[and]]wherein

a voltage level of the second internal voltage is lower than the voltage level of an external supply voltage.

2. (Canceled)

3. (Original) The semiconductor memory device of claim 1, wherein the voltage level of the second internal voltage is different from the level of an operating voltage of the semiconductor memory device.

4. (Currently Amended) A semiconductor memory device, comprising: ~~having~~

an output driver in which a first NMOS transistor and a second NMOS transistor are connected in series, the drain of the first NMOS transistor is connected to an output pad, and the

source of the second NMOS transistor is connected to a ground voltage[[,]]; and

~~having~~ a driving circuit which applies a driving voltage to the gate of the second NMOS transistor in response to data[[,]] and an internal supply voltage[[,]]; wherein

a ground voltage level of the driving circuit is higher than the voltage level of the ground voltage to which the source of the second NMOS transistor is connected.

5. (Original) The semiconductor memory device of claim 4, wherein the voltage level of the driving voltage is different from the level of an operating voltage of the semiconductor memory device.

6. (Original) The semiconductor memory device of claim 4, wherein the voltage level of the driving voltage is lower than the voltage level of an external supply voltage.

7. (Currently Amended) A semiconductor memory device, comprising: ~~having~~

an output driver in which a first NMOS tansistor and a second NMOS transistor are connected in series, the drain of the first NMOS transistor is connected to an output pad, and the source of the second NMOS transistor is connected to a ground voltage[[,]]; and

~~having~~ a precharge transistor, the source of which ~~the source~~ is connected to a connection node of the first NMOS transistor and the second NMOS transistor and the drain of which ~~drain~~ is connected to a supply voltage[[,]]; wherein

the precharge transistor is connected to ~~includes~~ a voltage compensating circuit for lowering the rise in the voltage level of the connection node due to the rise in the voltage level of the gate of the first NMOS transistor.

8. (Original) The semiconductor memory device of claim 7, wherein the voltage compensating circuit comprises a capacitor which is connected between the gate and the source of the precharge transistor.

9. (Original) The semiconductor memory device of claim 8, wherein the capacitor has the same capacitance as a coupling capacitor between the gate and the source of the first NMOS transistor.

10. (Original) The semiconductor memory device of claim 7, wherein the precharge transistor is an NMOS transistor.